

Semiconductor Device and Method of Manufacturing a Semiconductor Device

BACKGROUND OF THE INVENTION

1. Field Of the Invention:

The present invention relates to the technical field of semiconductor devices, and in particular to the structure of surge protective component.

2. Description of Related Art:

In the related art, two terminal surge protective components are widely used as semiconductor devices for protecting electronic circuits from surge voltages occurring due to lightening strikes, etc.

Numeral 101 in FIG. 8 is an example of a semiconductor device of the related art. Here, P-type base layers 113a and 113b are provided at a portion in the vicinity of both the inner side surface and the reverse side surface of an N-type substrate 109 so that a PN junction is formed between the substrate 109 and the base layers 113a and 113b.

The base layers 113a and 113b are positioned substantially in the vicinity of the center of the semiconductor device 101, and are patterned so as to be rectangular in shape, with rounded corners. N-type emitters 122a and 122b are arranged at a part in the vicinity of the surface of the inside of the base layers 113a and 113b so that a PN junction is formed between each of

the emitter layers 122a and 122b and the base layers 113a and 113b.

Ohmic layers 121a and 121b with a high P-type surface concentration are provided at a portion where the emitter
5 layers 122a and 122b provided in the vicinity of the surface on the inside of the base layers 113a and 113b are not provided.

Metal films 127a and 127b are formed at the surfaces of the emitter layers 122a and 122b and the ohmic layers 121a and 121b on the surface side and rear surface side of the substrate
10 109. The metal film 127a at the surface side is electrically connected to the surface side emitter layer 122a and the ohmic layer 121a, but is not connected to the substrate 109. The metal film 127b of the rear surface side is electrically connected to the surface side emitter layer 122b and the ohmic layer 121b,
15 but is not connected to the substrate 109.

The semiconductor device 101 of this structure has a four-layer PNP structure when viewed from the surface side or from the rear side. This means that the PN junction between the base layers 113a and 113b and the substrate 109 is reverse
20 biased for whichever of the metal films 127a and 127b a voltage is applied to, wherein a current flows as a result of this PN junction experiencing an avalanche breakdown.

When a current flows, the PNP structure latches up, and a voltage state lower than a voltage during avalanche breakdown
25 is maintained between the metal films 127a and 127b. Therefore,

when the semiconductor device 101 is connected in parallel with an electronic circuit, when a surge voltage is applied to the electronic circuit, the semiconductor device 101 conducts in such a manner that the surge voltage is not applied to the electronic circuit.

There are, however, drawbacks with this semiconductor device 101 in that the PN junction formed between the base layers 113a and 113b and the substrate 109 are easily destroyed and reliability therefore becomes poor.

In order to improve the reliability of the semiconductor device 101, there has been proposed a structure where a high-concentration N-type layer is provided within the substrate 110 so that a PN junction is formed between the N-type layer and base layers 113a and 113b. However, this requires a complex process because the N-type layer is buried more deeply than the base layers 113a and 113b.

As the present invention sets out to resolve the problems encountered in the related art, it is the object of the present invention to provide a surge protection semiconductor device that has a straightforward manufacturing process, a simple structure, and is highly reliable.

SUMMARY OF THE INVENTION

In order to resolve the aforementioned problems, a semiconductor device of the present invention having, when one

of either an N-type or P-type is defined as a first conductivity type, and the other is defined as a second conductivity type, a semiconductor substrate of the first conductivity type, comprises first and second buried layers (in this invention,

5 a buried layer may include a layer being partially exposed on the surface of a semiconductor substrate 9 as shown in Fig.

6) provided within the semiconductor substrate, being of the first conductivity type, and being of a higher concentration than the semiconductor substrate, first and second emitter layers of the first conductivity type, first and second base layers of the second conductivity type, and a substrate layer constituted by the semiconductor substrate. The substrate layer is sandwiched between the first and second buried layers.

At least a part of the first and second base layers are positioned on one side surface and the other side surface of the semiconductor substrate so as to form PN junctions with the first and second buried layers. At least a part of the first and second emitter layers are located in a vicinity of a surface inside of the first and second base layers so as to form PN junctions with the first and second base layers.

The first and second base layers are respectively provided between the first and second emitter layers and the first and second buried layers, and the first and second buried layers are located between the first and second base layers and the substrate layer.

With this semiconductor device of the present invention,
the first and second metal films are formed on both sides of
the semiconductor substrate, the first emitter layer and the
first base layer are electrically short-circuited by the first
5 metal film; and the second emitter layer and the second base
layer are electrically short-circuited by the second metal
film.

Further, with the semiconductor device of this invention,
ring-shaped first and second moats with bottom surfaces
10 reaching the buried layers are formed on both sides of the
semiconductor substrate and the first and second emitter layers
are located on inside of the first and second moats.

The insides of the first and second moats of this
semiconductor device of the present invention are filled with
15 oxide.

Moreover, at least a part of the first and second base
layers are positioned at a region on outside of the first and
second moats of surfaces of the semiconductor substrate.

Still further, at least a part of the first and second
20 buried layers are positioned at a region on the outside of the
first and second moats of the surfaces of the semiconductor
substrate of the semiconductor device of the present invention.

A semiconductor device manufacturing method of the present
invention comprises the steps of, when one of an N-type and
25 P-type is defined as a first conductivity type and the other

is defined as a second conductivity type:

forming a first buried layer of the first conductivity type in the vicinity of the surface at the inside of one side of the semiconductor substrate of the first conductivity type and forming a second buried layer of the first conductivity type in a vicinity of the surface of the other side, in such a manner that the first and second buried layers sandwich a substrate layer composed of a remaining portion of the semiconductor substrate, forming first and second base layers of the second conductivity type in the vicinity of surfaces at insides of the first and second buried layers in such a manner that bottom surfaces are positioned in the first and second buried layers; and forming first and second emitter layers of the first conductivity type in the vicinity of surfaces at insides of the first and second base layers so that the bottom surfaces thereof are positioned in the first and second base layers.

In the semiconductor device manufacturing method of the present invention, the first and second buried layers are formed by introducing an impurity of the first conductivity type into the semiconductor substrate with the surfaces of both sides of the semiconductor substrate completely exposed and diffusing impurity of the first conductivity type.

Further, in the semiconductor device manufacturing method of the present invention, the first and second base layers are

formed by introducing an impurity of the second conductivity type into the first and second buried layers with the surfaces of the first and second buried layers completely exposed and diffusing impurity of the second conductivity type.

5 Moreover, the semiconductor device manufacturing method of the present invention further comprises a step of, with ring-shaped moats having bottom surfaces reaching positions deeper than the bottom surfaces of the base layers, forming moats including the first and second emitter layers inside of
10 the ring-shaped moats on both sides of the semiconductor substrate.

Further, the semiconductor device manufacturing method of the present invention may comprise a further step of forming first and second metal films short-circuiting the first and
15 second emitter layers positioned inside of the ring-shaped moats and the first and second base layers after filling the insides of the first and second moats with oxide and forming first and second passivation films.

20 BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(a) to FIG. 1(k) illustrate steps for manufacturing a semiconductor device of a first example of the present invention.

FIG. 2 is a view (first of two) illustrating a structure
25 for emitter layers of this semiconductor device.

FIG. 3 is a view (second of two) illustrating a structure for emitter layers of this semiconductor device.

FIG. 4(a) and FIG. 4(b) are views illustrating the planar shape of this semiconductor device.

5 FIG. 5(a) to FIG. 5(d) illustrate steps for manufacturing a semiconductor device of a second example of the present invention.

FIG. 6 is a view illustrating a structure for emitter layers of this semiconductor device.

10 FIG. 7(a) and FIG. 7(b) are views illustrating the planar shape of this semiconductor device.

FIG. 8 is a view illustrating a surge protective component of the related art.

15 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The semiconductor device of the present invention is a two terminal semiconductor device used for protecting electronic circuits from surge voltages. The semiconductor device includes, when one of either an N-type or P-type is defined as a first conductivity type and the other is defined as a second conductivity type, a semiconductor substrate of the first conductivity type, first and second buried layers provided within the semiconductor substrate, being of the first conductivity type, and being of a higher concentration than
20 the semiconductor substrate, first and second emitter layers
25

of the first conductivity type, first and second base layers of the second conductivity type, and a substrate layer constituted by the semiconductor substrate. The semiconductor layer is sandwiched between the first and second buried layers; and the first and second base layers are positioned on one side surface and the other side surface of the semiconductor substrate so as to form PN junctions with the first and second buried layers. The first and second emitter layers are located in the vicinity of the surface of the inside of the first and second base layers so as to form PN junctions with the first and second base layers; and the first and second base layers are respectively provided between the first and second emitter layers and the first and second buried layers, while the first and second buried layers are located between the first and second base layers and the substrate layer.

The first and second buried layers are formed by means of introducing impurities to within the semiconductor substrate with the surface side and rear surface side of the semiconductor being completely exposed. Processing to pattern the first and second buried layers is therefore unnecessary.

The first and second base layers are arranged so as to be positioned in the vicinity of the inside surfaces of the first and second buried layers so that the first and second base layers form PN junctions between the first and second buried layers and a PN junction is not formed between the first

and second base layers and the substrate layer.

The first and second base layers are formed in such a manner that the entire surfaces of the first and second buried layers are exposed. When inner portions of first and second moats are then separated from the cross-section of the semiconductor device by the ring-shaped first and second moats with the bottom parts of the first and second base layers reaching the first and second buried layers, there are no spherical or cylindrical junction portions at the PN junction formed between the first and second base layers and the first and second buried layers; and this junction therefore consists only of a planar junction.

Further, when the first and second base layers are formed partially within the first and second buried layers, spherical junction portions and circular junction portions of a PN junction formed between the first and second base layers and the first and second buried layers are eliminated by the first and second moats so that only planar junction portions remain.

In either of these cases, the ends of a PN junction formed between the first and second base layers and the first and second buried layers are exposed within the first and second moats, but are not exposed at the surface of the semiconductor substrate.

The inside of the first and second moats is filled up with oxide etc. and baked so as to form first and second passivation films without causing the electrical characteristics of the

PN junction to deteriorate. The oxide may include glass granules comprising lead oxide, aluminum oxide, silicon oxide etc.

A surge protective component of a preferred embodiment of a semiconductor device of the present invention and a method of manufacturing this surge protective component will now be described using the drawings.

FIG. 1(a) to FIG. 1(k) are views showing processes illustrating the method of manufacturing a semiconductor device of a first example of the present invention. Here, the first conductivity type is an N-type (including N⁻, N⁺ and N⁺⁺ types) and the second conductivity type is a P-type (including P⁻, P⁺ and P⁺⁺-types).

Referring to FIG. 1(a), first, a semiconductor substrate 9 consisting of high-resistivity N-type silicon single crystal is prepared. Here, a crystal with a resistivity of 20Ωcm or more, and less than or equal to 60Ωcm (less than or equal to $2 \times 10^{14}\text{cm}^3$ and greater than or equal to $7 \times 10^{13}\text{cm}^3$ in concentration conversions) was used as the semiconductor substrate 9.

Next, phosphorous is implanted in with the entire surfaces of both sides of the semiconductor substrate 9 exposed; and as shown in FIG. 1(b), high concentration N-type layers 11a and 11b are formed in the vicinity of the surfaces of both of the inner surfaces of the semiconductor substrate 9.

Next, as shown in FIG. 1(c), impurities contained in the high-concentration N-type layers 11a and 11b are diffused through heat processing so that first and second buried layers 12a and 12b of higher surface concentrations than the concentration of the semiconductor substrate 9 are formed. In this state, the surface of the first and second buried layers 12a and 12b coincide with the surface of the semiconductor substrate 9; and the depth of diffusion is substantially equal along the whole of the region for the first and second buried layers 12a and 12b.

Numeral 10 in FIG. 1(c) indicates a substrate layer 10 constituting a low N-type concentration portion, such portion being a portion of the semiconductor substrate 9, except the first and second buried layers 12a and 12b.

In this situation, the first and second buried layers 12a and 12b are formed over both surfaces of the semiconductor substrate 9 in their entireties; and therefore sandwich the substrate layer 10. Numerals 19a and 19b show silicon oxide films formed on the surfaces of the buried layers 12a and 12b during a diffusion process.

Next, the silicon oxide films 19a and 19b are removed and boron is implanted into the vicinity of the surfaces of the inner parts of the first and second buried layers 12a and 12b on the front and rear surfaces with the surfaces of the first and second buried layers 12a and 12b in an exposed state, as shown

in FIG. 1(d). High-concentration P-type layers 14a and 14b are formed over the entire surfaces of the first and second buried layers 12a and 12b. In this state, the first and second buried layers 12a and 12b are buried in lower layers of the high-concentration P-type layers 14a and 14b.

Next, when boron constituting the high-concentration P-type layers 14a and 14b is diffused by subjection to heat processing over a prescribed period of time, P-type first and second base layers 13a and 13b are formed in the vicinity of the inner part of both surfaces of the semiconductor substrate 9, as shown in Fig. 1(f).

As a result of this diffusion processing and diffusion processing described later, the positions of the bottom parts of the first and second base layers 13a and 13b exceed the bottom parts of the first and second buried layers 12a and 12b without being deep; and the first and second base layers 13a and 13b connect with the upper parts of the first and second buried layers 12a and 12b at this bottom part. The first and second base layers 13a and 13b therefore do not connect with the substrate layer 10.

In this state, at the inner part of the semiconductor substrate 9, the first and second buried layers 12a and 12b are positioned on either side of the substrate layer 10; and the first and second base layers 13a and 13b are positioned at the side surfaces of the first and second buried layers 12a

and 12b. PN junctions are formed between the first and second base layers 13a and 13b and the first and second buried layers 12a and 12b.

The surface of the first and second base layers 13a and 13b and the surface of the semiconductor substrate 9 coincide; and the first and second buried layers 12a and 12b are not exposed at the surface of the semiconductor substrate 9 because the first and second buried layers 12a and 12b are sandwiched by the first and second base layers 13a and 13b and the substrate layer 10.

Numerals 19a and 19b in FIG. 1(e) show silicon oxide films formed on the surfaces of the base layers 13a and 13b during the diffusion process, and silicon oxide films 19a and 19b are positioned on both sides of the semiconductor substrate 9.

An opening of a large surface area is made at prescribed positions on the silicon oxide films 19a and 19b on the surfaces on both sides of the semiconductor substrate 9 using photographic processes and etching processes. After exposing the surfaces of the base layers 13a and 13b, boron is implanted into this exposed portion and a high-concentration P-type layer is formed. The numerals 15a and 15b in FIG. 1(f) indicate openings of a large surface area formed at the silicon oxide films 19a and 19b. Numerals 16a and 16b indicate high P-type concentration layers formed at the bottom surfaces of the openings 15a and 15b.

Next, mesh-like openings are made in the planar pattern at positions where the high P-type concentration layers 16a and 16b of the silicon oxide films 19a and 19b on both sides are not formed. The surfaces of the base layers 13a and 13b are then exposed, phosphorous is introduced, and a high N-type concentration layer is formed. Numerals 17a and 17b in FIG. 1(g) indicate mesh-like openings formed respectively at the silicon oxide films 19a and 19b on both sides and numerals 18a and 18b indicate high-concentration N-type layers formed at the bottom surfaces of the openings 17a and 17b. The planar shape of the high N-type concentration layers 18a and 18b is mesh-like.

In this state, high-concentration P-type layers 16a and 16b and high-concentration N-type layers 18a and 18b are both formed in the vicinity of the inner surfaces of the base layers 13a and 13b.

Next, the high-concentration P-type layers 16a and 16b and the high-concentration N-type layers 18a and 18b are diffused by heating. FIG. 1(h) shows the situation after diffusion where the silicon oxide films formed during diffusion processing are removed. Here, first and second ohmic layers 21a and 21b are formed by diffusion of the high P-type concentration layers 16a and 16b; and first and second emitter layers 22a and 22b are formed by diffusion of the high-concentration N-type layers 18a and 18b.

The depth of diffusion of the first and second ohmic layers 21a and 21b and the first and second emitter layers 22a and 22b is shallower than that of the first and second base layers 13a and 13b so that the first and second ohmic layers 21a and 21b and the outer portion of the surface shape of the first and second emitter layers 22a and 22b are located further towards the inside than the outer portion of the surface shape of the first and second base layers 13a and 13b.

The first and second ohmic layers 21a and 21b and the first and second emitter layers 22a and 22b are formed on the insides of the first and second base layers 13a and 13b, respectively.

A PN junction is therefore formed between the first and second emitter layers 22a and 22b and the first and second base layers 13a and 13b because these layers are of opposite conductivity types.

On the other hand, the first and second ohmic layers 21a and 21b and the first and second emitter layers 22a and 22b do not make contact with the first and second buried layers 12a and 12b or with the substrate layer 10.

The pattern on one side of the semiconductor substrate 9 and on the other side is substantially the same in this state. This planar shape is shown in FIG. 4(a). The first and second emitter layers 22a and 22b are formed in the shape of a mesh. This means that the surfaces of the first and second base layers 13a and 13b are exposed in dotted state within the region where

the surfaces of the first and second emitter layers 22a and 22b are positioned.

FIG. 1(h) is a cross-section of a portion that does not include the first and second base layers 13a and 13b in a dotted state, corresponding to a cross-section taken along line A-A of FIG. 4(a). FIG. 2 is a cross-section of a portion that includes the surfaces of the first and second base layers 13a and 13b in a dotted state that corresponding to a cross-section taken along line B-B of FIG. 4(b).

Next, as shown in the situation in FIG. 1(h) and FIG. 2, resist films having ring-shaped openings are formed on the front and rear surfaces of the semiconductor substrate 9, the semiconductor substrate 9, with the bottom surfaces of the openings exposed, is etched, and moats are formed.

In FIG. 1(i), after moats are formed by etching, the situation is such that the resist film is removed. Here, numeral 25a shows a first moat formed at one side surface of the semiconductor substrate 9 and numeral 25b shows a second moat formed in the surface on the other side.

The ring-shaped openings of the resist films are located along a boundary of the first and second emitter layers 22a and 22b and the first and second base layers 13a and 13b, and the boundary of the first and second ohmic layers 21a and 21b and the first and second base layers 13a and 13b.

In other words, the ring-shaped openings of the resist

films are positioned above the edge portions of a region constituted by the first and second ohmic layers 21a and 21b and the first and second emitter layers 22a and 22b. The first and second moats 25a and 25b are formed in the same ring shape as the pattern for the openings for the resist films and are positioned above the edge portions of regions constituted by the first and second ohmic layers 21a and 21b and the first and second emitter layers 22a and 22b. That is, the first and second emitter layers 22a and 22b and the first and second ohmic layers 21a and 21b are positioned to the inside of the rings of the first and second moats 25a and 25b.

The first and second moats 25a and 25b are deeper than the depth of the PN junction formed by the first and second base layers 13a and 13b and the first and second buried layers 12a and 12b; and therefore, the first and second moats 25a and 25b are only dug to depths that do not reach the substrate layer 10. The bottom parts of the first and second moats 25a and 25b are positioned in the first and second buried layers 12a and 12b. Therefore, an inner region and outer region of the first and second moats 25a and 25b of the first and second base layers 13a and 13b are electrically separated by the PN junction formed between the first and second base layers 13a and 13b and the first and second buried layers 12a and 12b.

The PN junction formed between the first and second base layers 13a and 13b on the inside of the first and second moats

25a and 25b and the first and second buried layers 12a and 12b is therefore a planar junction.

Next, oxide is affixed to both sides of the semiconductor substrate 9 and an inside portion of a ring for the first and second moats 25a and 25b (and a scribe line portion for the semiconductor substrate 9 (not shown)) are exposed using photographic and etching processes after baking.

In this state, as shown in FIG. 1(j), first and second passivation films 26a and 26b are formed by silicon oxide that fills up the inside of the first and second moats 25a and 25b and silicon oxide positioned at the surface of the region on the outside of the first and second moats 25a and 25b.

Next, as shown in FIG. 1(k), a first metal film 27a consisting of a metal such as nickel is formed at the surface of the first ohmic layer 21a and first emitter layer 22a on one side of the semiconductor substrate 9. On the other side, a second metal film 27b of the same substance as the first metal film 27 is formed at the surface of the second ohmic layer 21b and the second emitter layer 22b so as to subsequently form the semiconductor device 1 of the present invention.

The surface concentration of the first and second ohmic layers 21a and 21b is higher than the concentration of the surfaces of the first and second base layers 13a and 13b. When the first and second metal films (described later) are formed at the surface of the first and second ohmic layers 21a and

21b and the first and second emitter layers 22a and 22b, the first and second metal films are ohmically connected with the first and second ohmic layers 21a and 21b, and the first and second metal films are therefore electrically connected with the first and second base layers 13a and 13b via the first and second ohmic layers 21a and 21b.

The first and second metal films and the first and second emitter layers 22a and 22b are ohmically connected because the surface concentrations of the first and second emitter layers 22a and 22b are sufficiently high.

The bottom parts of the first and second ohmic layers 21a and 21b and the first and second emitter layers 22a and 22b do not make contact with the first and second buried layers 12a and 12b.

A plan view of the front surface and rear surface in the state, where the first and second passivation films 26a and 26b and the first and second metal films 27a and 27b are peeled, (i.e., in the same state as shown in FIG. 1(i)) is shown in FIG. 4(b). FIG. 3 is a cross-sectional view taken along line B-B in FIG. 4(b).

With the semiconductor device 1 of the present invention, the concentration of the first and second buried layers 12a and 12b is higher than the concentration of the substrate layer 10; and these layers have a resistivity of 4 to 6 Ω cm. The withstand voltage of the PN junction formed between the first

and second base layers 13a and 13b; and the first and second buried layers 12a and 12b is therefore low at approximately 200 to 500 Volts.

The depth of the first and second base layers 13a and 13b is approximately 20 to 30 μ m and the depth of the first and second buried layers 12 is 30 to 40 μ m. The thickness of the substrate layer 10 is approximately 200 to 300 μ m.

At the semiconductor device 1, the first and second base layers 13a and 13b and the substrate layer 10 do not make contact; and a PN junction is therefore not formed between them.

A PN junction having a large surface area and low withstand voltage is formed between the first and second base layers 13a and 13b and the first and second buried layers 12a and 12b. Therefore, when a surge voltage is applied so that the semiconductor device 1 conducts, a current flows in the PN junction formed between the first and second base layers 13a and 13b and the first and second buried layers 12a and 12b in a uniform manner without this current partially converging; and resistance to destruction is therefore high.

Further, the PN junction, formed between the first and second base layers 13a and 13b and the first and second buried layers 12a and 12b, is only a planar junction and no spherical junctions or cylindrical junctions exist. There are therefore no portions within the PN junction where the withstand voltage is low and current convergence therefore does not occur.

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The first and second buried layers 12a and 12b are formed by diffusion from the surface of the semiconductor substrate 9 and are therefore of a high concentration. The avalanche breakdown voltage of the PN junction between the first and second base layers 13a and 13b and the first and second buried layers 12a and 12b can therefore be easily controlled.

Manufacture can be completed with few photographic processes because the first and second base layers 13a and 13b and the first and second buried layers 12a and 12b are not patterned.

The present invention does, however, also include semiconductor devices where the first and second base layers 13a and 13b are patterned.

The manufacturing processes for this semiconductor device are now described in a second embodiment of a semiconductor device of the present invention, with the diffusion layers and thin films being the same as those for the semiconductor device of the first example and with all items being given the same numerals.

First, FIG. 5(a) is a view corresponding to FIG. 1(e). Referring to FIG. 5(a), points of difference with the above embodiment are that the P-type first and second base layers 33a and 33b are positioned at the centers of the first and second buried layers 12a and 12b and are partially arranged in the vicinity of the surface of the inside thereof. The surfaces

of the first and second base layers 33a and 33b and the surfaces of the first and second buried layers 12a and 12b are also exposed at the surfaces of the semiconductor substrate 9.

FIG. 5(a) shows the situation when silicon oxide films 19a and 19b are formed at the surfaces of the first and second base layers 33a and 33b and the surfaces of the first and second buried layers 12a and 12b.

The planar shapes of the first and second base layers 33a and 33b are in the shape of quadrilaterals with rounded corners, with first and second buried layers 12a and 12b remaining at portions at the periphery of the first and second base layers 33a and 33b at the surfaces of the semiconductor substrate 9.

P-type and N-type impurities are implanted into portions in the vicinity of the surface at the inside surfaces of the first and second base layers 33a and 33b are diffused. P⁺ type first and second ohmic layers 21a and 21b and N⁺ type first and second emitter layers 22a and 22b are then formed, as shown in FIG. 5(b).

FIG. 7(a) shows the condition of both sides of the semiconductor substrate 9 in this state. FIG. 5(b) corresponds to a cross-sectional view taken along line C-C of FIG. 7(a).

When first and second moats 25a and 25b are formed along exposed edge portions of the surface of the semiconductor substrate 9 of the first and second base layers 33a and 33b (i.e., along portions of the PN junction formed between the

first and second base layers 33a and 33b and the first and second buried layers 12a and 12b), exposed at the surface of the semiconductor substrate 9, as shown in FIG. 5(c), the first and second moats 25a and 25b form ring-shapes.

5 Cylindrical and spherical junction portions of a PN junction formed between the first and second base layers 33a and 33b and the first and second buried layers 12a and 12b by the first and second moats 25a and 25b are removed.

10 The first and second base layers 33a and 33b are therefore not arranged at the region on the outside of the first and second moats 25a and 25b and portions at the surfaces side of the first and second buried layers 12a and 12b are exposed.

15 Next, as shown in FIG. 5(d), oxide is baked so as to form first and second passivation films 26a and 26b at a surface portion of the first and second buried layers 12a and 12b, respectively, positioned at regions on the inside of the first and second moats 25a and 25b and on the outside of the first and second moats 25a and 25b.

20 Next, first and second metal films 27a and 27b are then formed on the inside of the first and second moats 25a and 25b with the surfaces of the first and second ohmic layers 21a and 21b and the first and second emitter layers 22a and 22b exposed in order to obtain a semiconductor device 2 of the present invention.

25 With this semiconductor device 2, the depths of the first

and second moats 25a and 25b are formed to be deeper than the depths of the first and second base layers 33a and 33b and spherical and cylindrical junction portions of the PN junction formed between the first and second base layers 33a and 33b
5 and the first and second buried layers 12a and 12b are removed by the first and second moats 25a and 25b.

The first metal film 27a is electrically connected to the first emitter layer 22a and the first ohmic layer 21a at a surface of one side of the semiconductor substrate 9; and the
10 second metal film 27b is electrically connected to the second emitter layer 22b and the second ohmic layer 21b at a surface on the other side.

FIG. 7(b) shows surface conditions for the front surface side and the rear surface side of the semiconductor 2 of the present invention with the first and second passivation films
15 26a and 26b and the first and second metal films 27a and 27b peeled away.

As with the semiconductor device 1 of the first embodiment, the planar shape of the first and second emitter layers 22a and 22b of this semiconductor device 2 is also mesh-shaped;
20 and portions where the first and second base layers 33a and 33b are exposed at the surface of a region where the first and second emitter layers 22a and 22b are located are in dotted state.

25 FIG. 5(c) is a cross-sectional view taken along a line

C-C not passing portions where the first and second base layers 33a and 33b exist. FIG. 6 is a cross-sectional view taken along line D-D passing portions where the first and second base layers 33a and 33b exist.

5 With the semiconductor device 2 of the second embodiment, the first and second base layers 33a and 33b and the substrate layer 10 also do not make contact and a PN junction is therefore not formed between them. Further, the PN junction formed between the first and second base layers 33a and 33b and the
10 buried layers 12a and 12b is a planar junction and no spherical junctions or cylindrical junctions exist. There are therefore no portions within the PN junction where the withstand voltage is low and current convergence does not occur.

In the above, a description is given where the first
15 conductivity type is taken to be an N-type and the second conductivity type is taken to be a P-type, but conversely, a P-type may be taken to be the first conductivity type and an N-type may be taken to be a second conductivity type. In this case, the semiconductor substrate is P-type, the first and
20 second buried layers are P⁺- type, the first and second base layers are N-type, the first and second emitter layers are P⁺-type, and the first and second ohmic layers are N⁺-type.

A component for protecting against highly destructive surges can be obtained with few photographic processes.